APPLICATION

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TITLE: METHOD FOR OPTIMIZING DECOUPLING
CAPACITOR DESIGN IN DELAY LOCKED LOOPS

APPLICANTS: Claude GAUTHIER, Brian AMICK,
Dean LIU and Pradeep TRIVEDI

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METHOD FOR OPTIMIZING DECOUPLING CAPACITOR DESIGN IN DELAY LOCKED LOOPS

Background of Invention

[0001]   To increase processor performance, clock frequencies used by microprocessors, often referred to as "CPUs", have increased. Also, as the number of circuits that can be used in a CPU has increased, the number of parallel operations has risen. Examples of efforts to create more parallel operations include increased pipeline depth and an increase in the number of functional units in super-scalar and very-long-instruction-word architectures. As processor performance continues to increase, the result has been a larger number of circuits switching at faster rates. Thus, from a design perspective, important considerations, such as power, switching noise, and signal integrity must be taken into account.

[0002]   Higher frequencies for an increased number of circuits also increase switching noise on the power supply. If the components responsible for carrying out specific operations do not receive adequate power in a timely manner, computer system performance is susceptible to degradation. The switching noise may have a local or global effect. Circuits that create large amounts of noise may be relatively isolated; however, they may also affect other circuits, possibly involving very complex interactions between the noise generation and the function of affected circuits. Thus, providing power to the components in a computer system in a sufficient and timely manner has become an issue of significant importance.

[0003]   As the frequencies of modern computers continue to increase, the need to rapidly transmit data between chip interfaces also increases. To accurately receive

data, a clock is often sent to help recover the data. The clock determines when the data should be sampled by a receiver's circuits.

[0004]   The clock may transition at the beginning of the time the data is valid. The receiver would prefer, however, to have a signal during the middle of the time the data is valid. Also, the transmission of the clock may degrade as it travels from its transmission point. In both circumstances, a delay locked loop, or DLL, can regenerate a copy of the clock signal at a fixed phase shift from the original.

[0005]   Figure 1 shows a section of a typical computer system component (10). Data (22) that is 'n' bits wide is transmitted from circuit A (20) to circuit B (40). To aid in the recovery of the transmitted data, a clock composed of a clock signal (30), or CLK, is also transmitted with the data. The circuits could also have a path to transmit data from circuit B (40) to circuit A (20) along with an additional clock (not shown). The clock signal (30) may transition from one state to another at the beginning of the data transmission. Circuit B (40) requires a signal temporally located some time after the beginning of the valid data. Furthermore, the clock signal (30) may have degraded during transmission. The DLL has the ability to regenerate the clock signal (30) to a valid state and to create a phase shifted version of the clock to be used by other circuits, for example, a receiver's sampling signal. The receiver's sampling signal determines when the input to the receiver should be sampled. The performance of a DLL is critically related to the stability of its voltage supply.

[0006]   One common performance measure for a DLL is jitter. Jitter is the time domain error from poor spectral purity of an output. In other words, the output plus a known phase shift, should track the input. In a repeated output pattern, such as a clock signal, a transition that occurs from one state to another that does not happen at the same time relative to other transitions is said to have jitter. Jitter is related to power supply noise.

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[0007]   Often, power supplied to a computer system component varies due to switching by active circuits, which in turn, affects the integrity of the component's output. Typically, this power variation results from parasitics between a power supply for the component and the component itself. These parasitics may lead to the component not receiving power (via current) at the exact time it is required. One approach used by designers to combat this performance-inhibiting behavior is introducing decoupling capacitance to a particular circuit by positioning one or more decoupling capacitors close to the component. These decoupling capacitors store charge from the power supply and distribute the charge to the component when needed. For example, if power received by a component from a power supply has noise, one or more decoupling capacitors will distribute charge to the component to ensure that the component is not affected by the power variation on the power supply. In essence, a decoupling capacitor acts as a local power supply for one or more specific components in a computer system.

[0008]   Figure 2 shows a section of a typical power supply network (100) of a computer system. The power supply network (100) may be representative of a single integrated circuit, or "chip", or equally an entire computer system comprising multiple integrated circuits. The power supply network (100) has a power supply (112) that provides a power supply line (114) and a ground line (116) through an impedance network Z_1 (118). The impedance network is a collection of passive elements that result from inherent resistance, capacitance, and/or inductance of physical connections. A power supply line (122, 123) and a ground line (124, 125) supply a circuit A (120) and circuit B (126), respectively. Power supply line (123) and ground line (125) also supply circuit C (130) through another impedance network Z_2 (128) and additional impedance networks and circuits, such as impedance network Z_n (132) and circuit N (134). The impedance network and connected circuits may be simulated so that the designer can better understand the behavior of how the circuits interact.

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[0009]   Still referring to Figure 2, circuit A (120), circuit B (126), circuit C (130), and circuit N (134) may be analog or digital circuits. Also, circuit A (120), circuit B (126), circuit C (130), and circuit N (134) may generate and/or be susceptible to power supply noise. For example, circuit C (130) may generate a large amount of power supply noise that affects the operation of both circuit B (126) and circuit N (134). The designer, in optimizing the performance of circuit B (126) and circuit N (134), requires an understanding of the characteristics of the power supply noise. By understanding the characteristics of the power supply noise, the designer has a foundation on which to use a variety of design techniques to minimize the amount of power supply noise. One such technique, as discussed above, is the addition of decoupling capacitance. For example, decoupling capacitor C_N (136) located between a power supply line (133) and a ground line (135) may be added to reduce power supply noise. The amount of capacitance, due to the large amount needed for some designs, is an issue of significant importance.

Summary of Invention

[0010]   According to one aspect of the present invention, a method for optimizing decoupling capacitance in a delay locked loop comprises inputting a representative power supply waveform having noise to a simulation of the delay locked loop, estimating jitter of the delay locked loop, adjusting an amount of decoupling capacitance, and repeating the inputting, estimating, and adjusting until the jitter falls below a selected amount.

[0011]   According to another aspect of the present invention, a computer system for optimizing decoupling capacitance in a delay locked loop comprises a processor; a memory, and software instructions stored in the memory adapted to cause the computer system to input a representative power supply waveform having noise to a simulation of the delay locked loop, estimate jitter of the delay locked loop,

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adjust an amount of decoupling capacitance, and repeat the input, estimate, and adjust until the jitter falls below a selected amount.

[0012]   According to another aspect of the present invention, a computer-readable medium having recorded thereon instructions executable by a processor, the instructions adapted to input a representative power supply waveform having noise into a simulation of a delay locked loop, estimate jitter of the delay locked loop, adjust an amount of decoupling capacitance, and repeat the input, estimate, and adjust until the jitter falls below a selected amount.

[0013]   Other aspects and advantages of the invention will be apparent from the following description and the appended claims.

Brief Description of Drawings

[0014]   Figure 1 shows a typical computer system component.

[0015]   Figure 2 shows a typical computer system power supply network.

[0016]   Figure 3 shows a delay locked loop circuit test arrangement.

[0017]   Figure 4 shows a flow process in accordance with an embodiment of the present invention.

[0018]   Figure 5 shows captured power supply waveforms in accordance with another embodiment of the present invention.

[0019]   Figure 6 shows a delay locked loop circuit in accordance with another embodiment of the present invention.

Detailed Description

[0020]   Embodiments of the present invention relate to a method for optimizing decoupling capacitance in a delay locked loop. Embodiments of the present invention further relate to a computer system for optimizing decoupling

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capacitance in a delay locked loop. Embodiments of the present invention also relate to a program executed on a computer for optimizing decoupling capacitance in a delay locked loop.

[0021]   More particularly, embodiments of the present invention relate to the use of a representative power supply waveform having noise as an excitation into a simulation of a delay locked loop. By using a representative power supply waveform having noise, a reasonably accurate estimate of jitter is determined. The estimate of jitter of the delay locked loop is used to optimize an amount of decoupling capacitance. The amount of decoupling capacitance may be adjusted; the simulation of the delay locked loop performed; and the jitter estimated until the jitter falls below a selected amount.

[0022]   In Figure 2, the impedance networks (118, 128, 132) may be very complex arrangements of passive elements. The impedances may be the result of, but not limited to, a power supply connection, bulk capacitors, printed circuit board planes, printed circuit board vias, ceramic capacitors, printed circuit board to chip package connections, chip package planes, chip package vias, chip package capacitors, chip package to chip bump or bond wire connections, chip local and global decoupling capacitors, and switching and non-switching circuit elements. A "chip package" for the purpose of this description of the invention may be any package that allows mounting an integrated circuit to a printed circuit board. An integrated circuit, or die, is also referred to as a "chip" in this description. Also, each of the circuits (120, 126, 130, 134) in Figure 2 may induce power supply noise on the impedance networks (118, 128, 132). The power supply noise characteristics can result from interactions between the circuits (120, 126, 130, 134) coupled with the impedance networks (118, 128, 132).

[0023]   For a designer to adequately determine the amount of decoupling capacitance needed, the behavior of the power supply noise must be understood.

A simulation model is desirable. The simulation model is input into a simulation tool so that a computer can calculate the effects of one or more input excitations. One example of a simulation tool is SPICE, which is an acronym for Simulation Program with Integrated Circuit Emphasis. Modeling a complex array of impedances is difficult, however. Furthermore, even if an accurate simulation model is created, the computing overhead necessary to simulate one or more circuits with the impedance model network may be too great.

[0024] In the absence of an accurate model, worst case simulations are often used. In Figure 3, a test arrangement (150) for a DLL (155) is shown. The DLL (155) is supplied by a DC power supply (153). The DLL (155) has, in this example, a clock input (152) comprising a square wave between 0 V and 3.3 V at a frequency that can be varied between 2.5 kHz and 400 MHz on signal line (157). The DLL output (160) is a delayed copy of the clock input (152). A measuring device (162) measures the variations between the clock input (152) and the DLL output (160). Ideally, the delay between the clock input (152) and the DLL output (160) at any single frequency should be constant; however, due to power supply noise, timing variations in the transition from one state to another of the DLL output (160) occur. To model the power supply noise, a square wave generator (154) supplies a 0.5 V peak-to-peak signal that is added to the DC power supply (153) at adder (156). The combined DC power supply (153) and square wave generator (154) output is supplied on power supply line (158) to an impedance network Z_N (159) that is composed of various parasitic elements. Impedance network Z_N (159) may affect the characteristics of the power supply on power supply line (158). Power supply line (161) supplies power from the impedance network Z_N (159) to the DLL (155). For example, the combined DC power supply (153) and square wave generator (154) output on power supply line (158) may represent a worst case condition on a printed circuit board. The parasitic elements in impedance network Z_N (159) may represent the path from the printed circuit board to the DLL (155).

By adding decoupling capacitance (164), the effect of the power supply noise may be minimized. The frequencies and voltages of the DC power supply (153), square wave generator (154), and clock input (152) may be changed to model different operating points.

[0025] In Figure 3, because the noise generated by the square wave generator (154) may exceed typical power supply noise, the amount of decoupling capacitance needed to reduce the jitter in the DLL output (160) to an acceptable level may be oversized. Adding additional decoupling capacitance (164) may not be needed in the actual design to meet the desired specifications.

[0026] In Figure 4, an exemplary flow process (170) in accordance with an embodiment of the present invention is shown. At (172), a power supply waveform having noise is captured. A power supply waveform having noise for the purpose of this description may be any power supply that has deviations from a designed voltage. This power supply waveform is captured at some particular location within a power supply network. Those skilled in the art will appreciate that the noise in the captured power supply waveform comes from a dominant source of noise. A circuit under design does not provide a substantial contribution to the noise in the captured power supply waveform. The power supply waveform having noise may be used to adequately represent a large portion of the power supply network and associated circuitry.

[0027] In Figure 2, for example, circuit C (130) may be the dominant source of noise. The DLL under design may be circuit N (134). By capturing a power supply waveform having noise between impedance networks Z_2 (128) and Z_n (132), a system response that represents a large portion of the power supply network and associated circuitry is used. For example, the power supply network and associated circuitry may include the power supply (112), impedance network Z_1 (118), circuit A (120), circuit B (126), circuit C (130), and impedance network

Z_2 (128). Because the dominant source (circuit C (130)) is included in the power supply network and associated circuitry, a simulation using the power supply waveform having noise, impedance network Z_n (132), circuit N (134), and decoupling capacitor C_N (136) is sufficient.

[0028]   With regard to simulating a CPU circuit, capturing a power supply waveform on a printed circuit board near the CPU is desirable. The captured power supply waveform will also contain noise as a result of activities on the printed circuit board by one or more circuits. The captured power supply waveform may be the result of physically measuring the voltage on the printed circuit board under operating conditions with measuring equipment. These operating conditions may include extreme conditions in an effort to capture a worst case power supply waveform having noise. These operating conditions may be the result of varying one or more of the following: temperature, voltage, frequency, and manufacturing process. The captured power supply waveform may also be the result of a simulation of some portion of the power supply network. For the purposes of this description, a representative power supply waveform comprises an approximation of an actual power supply waveform as occurs in a realistic system. By capturing the power supply waveform at an intermediate point in the power supply network, a division in design responsibilities and expertise is achieved. A power supply network designer may focus on design and simulation of a portion of the power supply network while a circuit designer may capture representative power supply signals at an appropriate location to be used as an input to their circuits.

[0029]   The captured power supply waveform is digitized at (174) to be input to a simulation program. The digitization may be a direct point by point representation. The digitization may also be a representative model of the waveform that may include a formulated representation in which an equation characterizes the power supply waveform having noise. Capturing and digitizing

the power supply waveform does not preclude the addition of circuits to model another portion of the power supply network not represented in the captured and digitized power supply waveform. This additional portion of the power supply network may be used between the captured power supply waveform and the circuit under design. At (176), elements may be added to the simulation to represent additional power supply network components. For example, a captured power supply signal may be captured on a printed circuit board; however, the circuit to be designed resides on an integrated circuit. At (176), the power supply network elements that may be added include, but are not limited to, connections (parasitics) between the printed circuit board and chip package, connections (parasitics) between the chip package and chip, and connections (parasitics) between the chip power supply network and circuit under design. These added elements may improve the modeling of the actual passive parasitics. At (178), the DLL under design along with decoupling capacitance is simulated using the digitized power supply waveform having noise captured from the printed circuit board at (174) and the parasitics from (176). At (178), the computational overhead of the simulation is reduced due to the input of the power supply waveform having noise being used instead of a portion of the power supply network that may contain a large number of elements. Also, the simulation of the DLL at (178) is more accurate because the digitized power supply waveform having noise is used instead of a square wave or other pessimistic estimate.

[0030]   As the results of the simulation are analyzed, a decision is made at (180) as to whether the results meet expectations. At (180), the results of the simulation must meet specifications; however, the designer may have guard band or design goal expectations that improve upon the specification. For example, the amount of jitter may be compared against a specification. If the expectations are not met, (182) is followed to modify the design and/or amount of the decoupling capacitance. (178), (180), and (182) are repeated until a satisfactory result occurs.

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For example, the amount of decoupling capacitance may be increased until the amount of jitter meets or improves upon a specification.

[0031]   Those skilled in the art will appreciate that the captured power supply waveform having noise may be obtained from probing a physical system, such as a printed circuit board, chip package, or chip, under various operating conditions. Operating conditions include, but are not limited to, temperature, voltage, frequency, and manufacturing (process) variations. Those skilled in the art will also appreciate that the captured power supply waveform having noise may be obtained from probing an integrated circuit under various operating conditions. Furthermore, those skilled in the art will appreciate that the power supply waveform having noise obtained from a physical system may be obtained from a location adjacent to an intended location of the DLL under various operating conditions. Those skilled in the art will further appreciate that using the power supply waveform having noise in place of a portion of the power supply network reduces the computational load when simulating the circuit.

[0032]   Those skilled in the art will appreciate that the captured power supply signal having noise may be obtained from simulation data of a modeled printed circuit board's parasitics under various operating conditions. Furthermore, those skilled in the art will appreciate that the captured power supply waveform having noise may be obtained from simulation data of a power supply network's parasitics that may include, but is not limited to, the motherboard power supply network, motherboard to integrated circuit connections, and/or integrated circuit power supply network under various operating conditions. Operating conditions include, but are not limited to, temperature, voltage, frequency, and manufacturing (process) variations. Those skilled in the art will further appreciate that the simulation of the circuit using the power supply waveform having noise may be dependent on various operating conditions. Those skilled in the art will also appreciate that the simulation tool used to capture the power supply waveform

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having noise does not have to be the same simulation tool used to simulate the circuit using the power supply waveform having noise.

[0033]   Those skilled in the art will appreciate that capturing the power supply signal having noise, whether from a physical system or simulation, may advantageously be obtained adjacent to an intended location of the DLL.

[0034]   Those skilled in the art will appreciate that the noise may be captured separately from the power supply waveform and combined to create the power supply waveform having noise.

[0035]   Those skilled in the art will appreciate that multiple power supply waveforms having noise may be used simultaneously, and the multiple power supply waveforms having noise may be connected to different locations on the power supply network. Those skilled in the art will further appreciate that the DLL and additional circuits may be used in the simulation at (178).

[0036]   Those skilled in the art will appreciate that the DLL may be analog, digital, or a combination of both types of circuits.

[0037]   In Figure 5, two captured power supply waveforms having noise (202, 204), in accordance with various embodiments of the present invention, are shown.   Both captured power supply waveforms start at time zero at approximately 1 V. At 10 ns, one or more circuits interacting with one or more impedance networks create noise on the power supply waveforms.   For power supply waveform (202), the effect is reduced compared to power supply waveform (204).   Depending on the needs of a circuit designer, either power supply waveform (202, 204) can be digitized or modeled, and operatively used as the power supply input to the circuit simulation.

[0038]   Those skilled in the art will appreciate that power supply waveform (202) and power supply waveform (204) may have been captured under different

operating conditions. Those skilled in the art will further appreciate that power supply waveform (202) and power supply waveform (204) may have been captured at different locations within the power supply network.

[0039] Figure 6 shows an exemplary circuit (300) in accordance with another embodiment of the present invention. A block diagram drawing of a DLL (301) is shown. The DLL (301) has an input of CLK_IN (302) that is used to create a phased output. CLK_IN (302) is used as an input to a voltage controlled delay line (360) and to a phase detector (310). The phase detector (310) measures whether the phase difference between CLK_IN (302) and an output (384) of the delay path is correct. An adjustment in the phase delay produces signals that control a charge pump, typically up (U) (311) or down (D) (313) pulses. The charge pump (330) adds or removes charge from a loop filter, shown as a bias generator (350), changing the DC value at the input of the bias generator (350). A DC value input to the biased generator (350) is the control voltage, V_{CTRL} (332). The charge pump (330) adjusts the voltage stored on a capacitor C1 (340) between V_{CTRL} (332) and a potential. The bias generator (350) produces the signals V_{BP} (352) and V_{BN} (354) that control the delay of the voltage controlled delay line (360). The voltage controlled delay line (360) may be implemented using current starved elements. This means that the delays are controlled by modifying the amount of current available for charging and discharging capacitances. The linearity of a voltage controlled delayed line's characteristics determines the stable range of frequencies over which the delayed lock loop can operate. The output (384) from the voltage controlled delay line (360) provides a phase delayed clock CLK_OUT to other circuits.

[0040] Still referring to Figure 6, a power supply waveform having noise has been determined from a power supply network and digitized. The power supply waveform having noise is operatively used either through direct digitization or appropriate modeling such as a formulated representation where an equation

describes the signal's characteristics. The power supply waveform having noise is input to an impedance network Z_M (390). The impedance network Z_M (390) supplies power to the DLL (301) through power supply line (392) and ground line (394). Simulating the DLL (301) with the representation of the power supply waveform having noise provides a technique to estimate jitter.

[0041] Jitter represents the perturbations that result in the intermittent shortening or lengthening of signal elements. For example, a steady clock input may be used as an input of CLK_IN (302) to the DLL (301). A piece-wise linear representation of the power supply waveform having noise (202) (in Figure 5) may be used to supply the impedance network Z_M (390). The power supply waveform having noise (202) may be acquired from a simulation of a printed circuit board from a dominant power supply noise source. The impedance network Z_M (390) represents additional impedances between the printed circuit board and the DLL (301) that is located on an integrated circuit. The power supply waveform having noise may disturb the output (384) from the voltage controlled delay line (360). Timing variations between the transition from one state to another state between the input of CLK_IN (302) to the DLL (301) and the output (384) from the voltage controlled delay line (360) represent jitter. The addition of properly located decoupling capacitance, such as decoupling capacitor C_M (396), helps reduce the amount of power supply noise, hence jitter. Optimization of the decoupling capacitance is based on jitter using the power supply waveform having noise. Because a realistic power supply waveform having noise is used, the DLL design and associated decoupling capacitance will not be over designed with respect to control of jitter. Also, the simulation can be completed in a reasonable amount of time; therefore, the DLL design and/or the decoupling capacitance may be modified in an iterative fashion to improve the system's performance.

[0042] Those skilled in the art will appreciate that a computer system is described for determining a representation of a power supply waveform having noise, using

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that representation to simulate a delay locked loop and decoupling capacitance, and estimating jitter in the delay locked loop.

[0043]   Those skilled in the art will appreciate that a computer-readable medium having recorded thereon instructions executable by a processor is described to determine a representation of a power supply waveform having noise, using that representation to simulate a delay locked loop and decoupling capacitance, and estimating jitter in the delay locked loop.

[0044]   Advantages of the present invention may include one or more of the following. In some embodiments, because a representation of a power supply signal having noise is used, a more accurate circuit simulation may be performed. Realistic results help alleviate costly over design. A circuit designed with more accurate power supply waveforms may require a reduced amount of decoupling capacitance, hence reduced chip area. The space saved due to the reduced chip area may be used for additional performance enhancing circuits, or may be used to reduce the final chip size, hence cost.

[0045]   In some embodiments, because a representation of a power supply signal having noise is used, a circuit simulation that requires less computational load may be performed.   Accordingly, more iterations in the design process may be afforded.

[0046]   In some embodiments, because a representation of a power supply signal having noise is used, tasks involved with designing a power supply network and individual circuits may be advantageously divided and performed by experts in their respective areas of expertise.

[0047]   While the invention has been described with respect to a limited number of embodiments, those skilled in the art, having benefit of this disclosure, will appreciate that other embodiments can be devised which do not depart from the

scope of the invention as disclosed herein. Accordingly, the scope of the invention should be limited only by the attached claims.